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Date: October 13, 2005 **Pages (including cover): 5**

To: **Issue/Publication Fee Branch** **Fax: 571-273-2885** **Ph:**

From: Donald R. Studebaker, Reg. No. 32,815 **Docket No. 031794-13**

Message: **The following documents are being presented for facsimile filing in the United States Patent and Trademark Office:**

1. Amendment Pursuant to 37 C.F.R. §1.312
2. Notice of Allowance and Issue Fee Transmittal – Part B (PTOL-85)
3. Permission to charge the **Deposit Account No. 19-2380** in the amount of **$1730.00** representing $1400..00 for Issue Fee, $300.00 Publication Fee and $30.00 for Advance Order of 10 Patent Copies.

In re Patent Application of
Inventor(s): Yoshimasa SEKINO
Application No. 10/811,836
Filed: March 30, 2004
For: **POWER-ON RESET CIRCUIT**

Due Date: **October 13, 2005**
Docket Number: 031794-13

Date: **October 13, 2005**
DRS/pt

CERTIFICATE OF FACSIMILE TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being facsimile transmitted to the USPTO at 571-273-2885, on **October 13, 2005.**

Signature:
Name: *Peaches Thomas*

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
Yoshimasa SEKINO	)	Group Art Unit: 2816
Serial No. 10/811,836	)	Examiner: Terry D. Cunningham
Filed: 3/30/2004	)	Confirmation: 3050
For: POWER-ON RESET CIRCUIT	)	October 13, 2005

AMENDMENT PURSUANT TO 37 C.F.R. §1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to issuance, please amend the above identified application as follows:

IN THE CLAIMS:

Please amend claim 3 as follows.

3. (Currently Amending) A power-on reset circuit comprising:

a first capacitor connected between a power supply line and a first node;

a first MOS transistor connected between said first node and a second node, and ON/OFF controlled based on a first pulse signal;

a second MOS transistor connected between said second node and a reference potential, and ON/OFF controlled based on a second pulse signal;

a second capacitor connected between said second node and said reference potential;

a timing control unit for generating said first and second pulse signals in synchronism with a clock signal externally applied thereto; and

an output portion outputting a reset signal when the potential of ~~said internal node~~ an